

LEAKAGE IN NANOMETER CMOS TECHNOLOGIES NARENDRA SIVA G CH ANDRAKASAN ANANTHA P %0A

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About Siva G. Narendra Anantha Chandrakasan is an associate professor of electrical engineering and computer science at the Massachusetts Institute of Technology. His research interests include the energy efficient implementation of DSPs, wireless microsensor networks, and CAD tools for VLSI.

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the device, circuit, and architecture levels of abstraction after first explaining the sensitivity of the various MOS leakage sources to

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Lecture 6 Leakage and Low-Power Design

Lecture 6 Leakage and Low-Power Design R. Saleh Dept. of ECE University of British Columbia res@ece.ubc.ca.

Sections of Chapter 2 and 3 in HJS Leakage is a big problem in the recent CMOS technology nodes A variety of leakage mechanisms exist in the DSM transistor

Statistical Modeling of Leakage in Nano-CMOS Circuits

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